



## SPICE Device Model NTHD5904T1

Dual N-Channel 2.5 V (G-S) MOSFET

### APPLICATION NOTE

#### CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro-Model (Sub-circuit)
- Level 3 MOS
- Applicable for both Linear and Switch Mode
- Applicable over a -55 to 125°C Temperature Range
- Models Gate Charge, Transient, and Diode Reverse Recovery Characteristics

#### DESCRIPTION

The attached SPICE Model describes typical electrical characteristics of the n-channel vertical DMOS. The sub-circuit model was extracted and optimized over a 25°C to 125°C temperature range under pulse conditions for 0 to 4.5 volts gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold. A novel gate-to-drain feedback capacitor network is used to model gate charge characteristics while avoiding convergence problems of switched  $C_{gd}$  model. Model parameter values are optimized to provide a best fit to measure electrical data and are not intended as an exact physical description of a device.

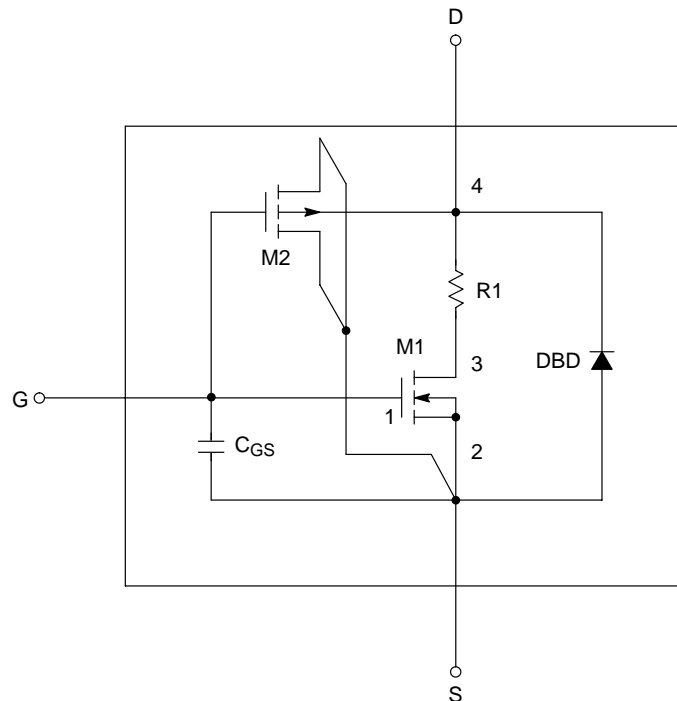


Figure 1. Model Sub-circuit

This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

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## MODEL EVALUATION

**N-CHANNEL DEVICE** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Test Conditions	Typical	Unit
<b>Static</b>				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	1.02	V
On-State Drain Current (Note 1.)	$I_{D(on)}$	$V_{DS} \geq 5.0 \text{ V}, V_{GS} = 4.5 \text{ V}$	32	A
Drain-Source On-State Resistance (Note 1.)	$r_{DS(on)}$	$V_{GS} = 4.5 \text{ V}, I_D = 3.1 \text{ A}$ $V_{GS} = 2.5 \text{ V}, I_D = 2.3 \text{ A}$	0.065 0.011	$\Omega$
Forward Transconductance (Note 1.)	$g_{fs}$	$V_{DS} = 10 \text{ V}, I_D = 3.1 \text{ A}$	7.0	S
Diode Forward Voltage (Note 1.)	$V_{SD}$	$I_S = 0.9 \text{ A}, V_{GS} = 0 \text{ V}$	0.8	V
<b>Dynamic (Note 2.)</b>				
Total Gate Charge	$Q_g$	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 3.1 \text{ A}$	3.2	nC
Gate-Source Charge	$Q_{gs}$		0.6	
Gate-Drain Charge	$Q_{gd}$		1.3	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10 \text{ V}, R_L = 10 \Omega, I_D \cong 1.0 \text{ A},$ $V_{GEN} = 4.5 \text{ V}, R_G = 6.0 \Omega$	11	ns
Rise Time	$t_r$		14	
Turn-Off Delay Time	$t_{d(off)}$		16	
Fall Time	$t_f$		20	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 0.9 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$	40	

1. Pulse test: pulse width  $\leq 300 \mu\text{s}$ , duty cycle  $\leq 2\%$ .
2. Guaranteed by design, not subject to production testing.

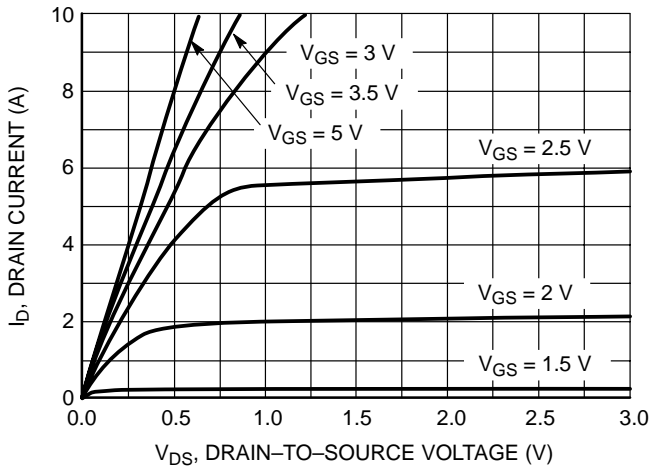


Figure 2. Drain Current vs. Drain-to-Source Voltage

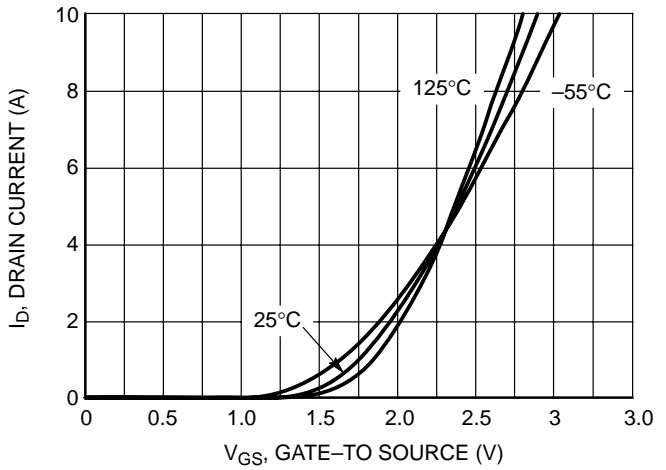


Figure 3. Drain Current vs. Gate-to-Source Voltage

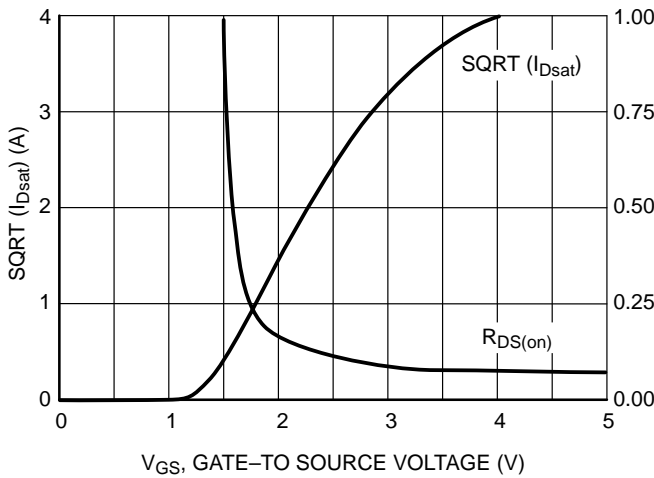


Figure 4. Sqrt vs. Gate-to-Source Voltage

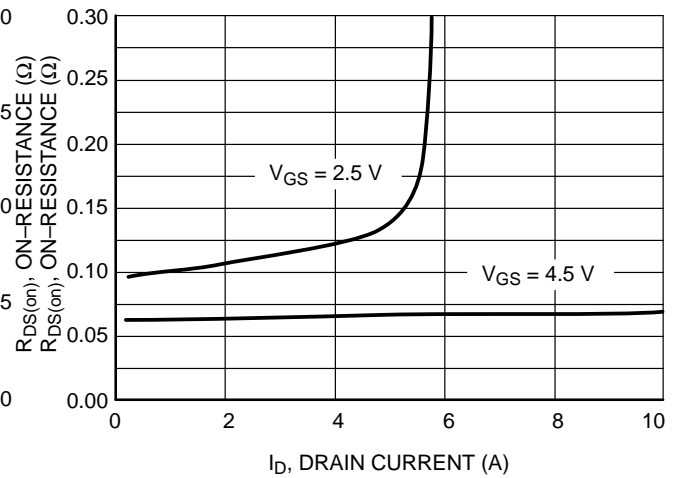


Figure 5. On-Resistance vs. Drain Current

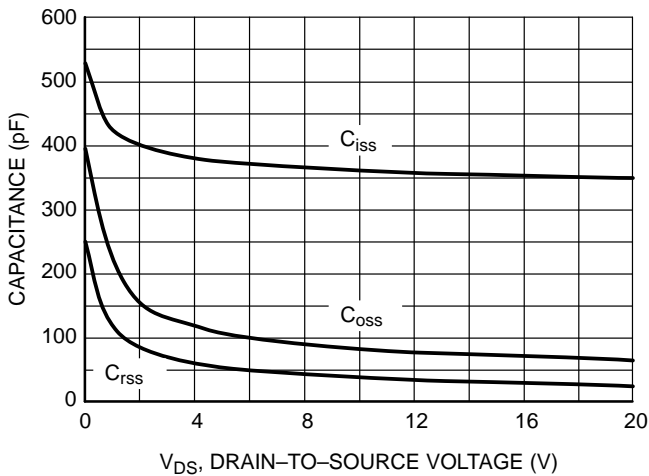


Figure 6. Capacitance vs. Drain-to-Source Voltage

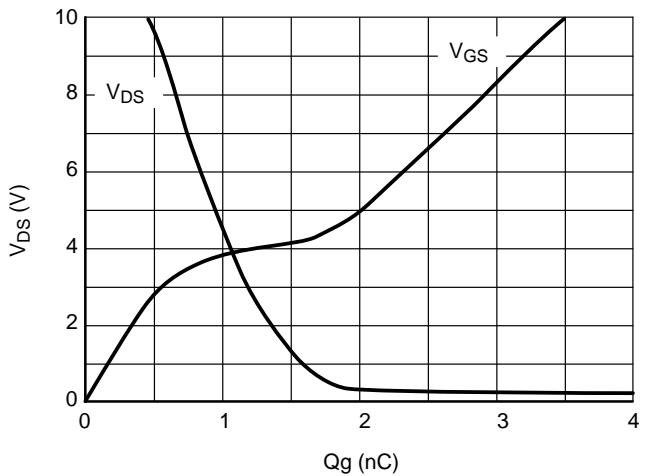


Figure 7.  $V_{DS}$  vs.  $Q_g$

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## H-SPICE

```
.SUBCKT Si5904DC 4 1 2
M1 3 1 2 2 NMOS W = 194914u L = 0.50u
M1 2 1 2 4 PMOS W = 194914u L = 0.95u
R1 4 3 RTEMP 260E-4
CGS 1 2 240E-12
DBD 2 4 DBD
*****
.MODEL NMOS NMOS (LEVEL = 3 TOX = 3E-8
+RS = 180E-4 RD = 0 NSUB = 1.57E17
+kp = 3.97E-5 UO = 650
+VMAX = 0 XJ = 5E-7 KAPPA = 1E-1
+ETA = 1E-4 TPG = 1
+IS = 0 LD = 0
+CGSO = 0 CGDO = 0 CGBO = 0
+TLEV = 1 BEX = -1.5 TCV = 2.8E-3
+NFS = 0.8E12 DELTA = 0.1)
*****
.MODEL PMOS PMOS (LEVEL = 3 TOX = 3E-8
+NSUB = 5E16 TPG = -1)
*****
.MODEL DBD D (CJO = 130E-12 VJ = 0.38 M = 0.31
+RS = 1 FC = 0.5 IS = 1E-5 TT = 17E-8 N = 1 BV = 40)
*****
.MODEL RTEMP R (TC1 = 6.5E-3 TC2 = 5.5E-6)
*****
.ENDS
```

P-SPICE


```
.SUBCKT Si5904DC 4 1 2
M1 3 1 2 2 NMOS W = 194914u L = 0.50u
M1 2 1 2 4 PMOS W = 194914u L = 0.95u
R1 4 3 RTEMP 260E-4
CGS 1 2 240E-12
DBD 2 4 DBD
*****
.MODEL NMOS NMOS (LEVEL = 3 TOX = 3E-8
+RS = 180E-4 RD = 0 NSUB = 1.57E17
+kp = 3.97E-5 UO = 650
+VMAX = 0 XJ = 5E-7 KAPPA = 1E-1
+ETA = 1E-4 TPG = 1
+IS = 0 LD = 0
+CGSO = 0 CGDO = 0 CGBO = 0
+NFS = 0.8E12 DELTA = 0.1)
*****
.MODEL PMOS PMOS (LEVEL = 3 TOX = 3E-8
+NSUB = 5E16 TPG = -1)
*****
.MODEL DBD D (CJO = 130E-12 VJ = 0.38 M = 0.31
+RS = 1 FC = 0.5 IS = 1E-5 TT = 17E-8 N = 1 BV = 40)
*****
.MODEL RTEMP R (TC1 = 6.5E-3 TC2 = 5.5E-6)
*****
.ENDS
```

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## I<sub>s</sub>-SPICE

```
.SUBCKT Si5904DC 4 1 2
M1 3 1 2 2 NMOS W = 194914u L = 0.50u
M1 2 1 2 4 PMOS W = 194914u L = 0.95u
R1 4 3 260E-4 RTEMP
CGS 1 2 240E-12
DBD 2 4 DBD
*****
.MODEL NMOS NMOS (LEVEL = 3 TOX = 3E-8
+RS = 180E-4 RD = 0 NSUB = 1.57E17
+kp = 3.97E-5 UO = 650
+VMAX = 0 XJ = 5E-7 KAPPA = 1E-1
+ETA = 1E-4 TPG = 1
+IS = 0 LD = 0
+CGSO = 0 CGDO = 0 CGBO = 0
+NFS = 0.8E12 DELTA = 0.1)
*****
.MODEL PMOS PMOS (LEVEL = 3 TOX = 3E-8
+NSUB = 5E16 TPG = -1)
*****
.MODEL DBD D (CJO = 130E-12 VJ = 0.38 M = 0.31
+RS = 1 FC = 0.5 IS = 1E-5 TT = 17E-8 N = 1 BV = 40)
*****
.MODEL RTEMP R (TC1 = 6.5E-3 TC2 = 5.5E-6)
*****
.ENDS
```

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